What is claimed is:

1. A motion estimation apparatus comprising:

a demultiplexer which receives a selection flag from a user and current image data, and selectively outputs the current image data using one output terminal selected from a plurality of output terminals by the selection flag;

a motion estimator which performs a motion estimation operation on the current image data using one motion estimation algorithm selected from a plurality of motion estimation algorithms depending on the output of the demultiplexer, and outputs a motion vector; and

a multiplexer which receives the selection flag and outputs the motion vector in response to the selection flag.

2. The apparatus of claim 1, wherein the plurality of motion estimation algorithms performed in the motion estimator includes a full search algorithm, a two-step hierarchical algorithm, a three-step hierarchical algorithm, and a four-step hierarchical algorithm.

3. The apparatus of claim 1, wherein the motion estimator comprises:

a first memory which stores the current image data and then outputs image data stored in an address input;

a second memory which stores previous image data and then outputs previous image data stored in an address input;

a data processor which receives the image data from the first and second memories and performs a motion estimation on the input image data; and

an address generation unit which provides an address command to each of the first and second memories.

4. The apparatus of claim 3, wherein the address generation unit determines an address to be output based on the selection flag input from the user.

5. The apparatus of claim 3, wherein the address generation unit comprises:

a controller;

a first selector which selectively outputs the selection flag input in response to a control signal generated by the controller using one of a plurality of output terminals;

an address generator which receives the selection flag from the first selector and then generates an address in response to the selection flag; and

a second selector which outputs the address generated by the address generator in response to a control signal generated from the controller.

6. The apparatus of claim 3, wherein the data processor has a plurality of unit data processors connected in parallel.

7. The apparatus of claim 6, wherein each of the plurality of unit data processors comprises:

a first register which stores and outputs the current image data;

a second register which stores and outputs row data of the previous image data;

a third register which stores and outputs column data of the previous image data;

a first multiplexer which selectively outputs the row data input from the second register or the column data input from the third register;

a substractor which calculates differences between the current image data input from the first register and the row data or column data of the previous image data input from the first multiplexer and outputs a result of the subtraction; and

an adder which adds an output of the substractor to previous values fed back to the adder and outputs an absolute value of a result of the adding.

8. The apparatus of claim 7 further comprising:

a fourth register and a fifth register which stores the outputs of the adder;

a second multiplexer which selectively feeds the outputs of the fourth register or the outputs of the fifth register back to the adder;

a third multiplexer which selectively outputs the outputs of the fourth register or the outputs of the fifth register; and

a sixth register which stores and outputs the outputs of the third multiplexer.